

FIG. 1

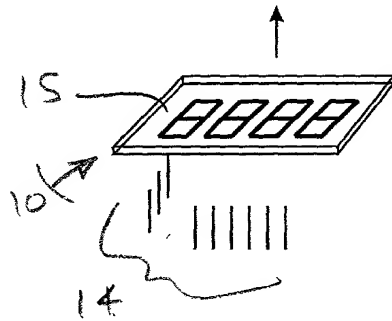
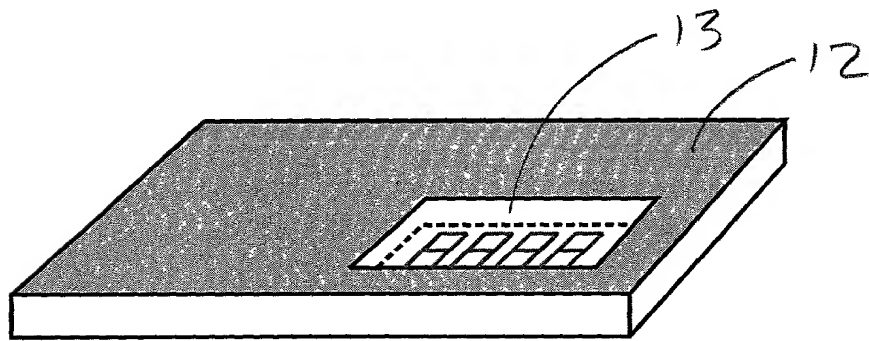


FIG. 2

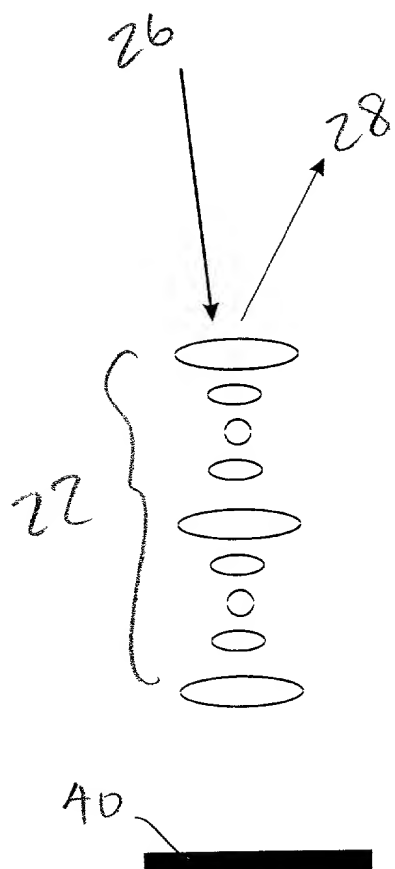


FIG. 3A

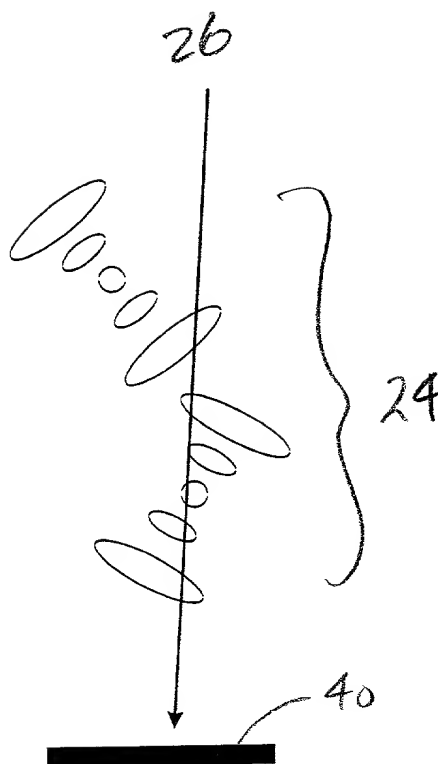


FIG. 3B

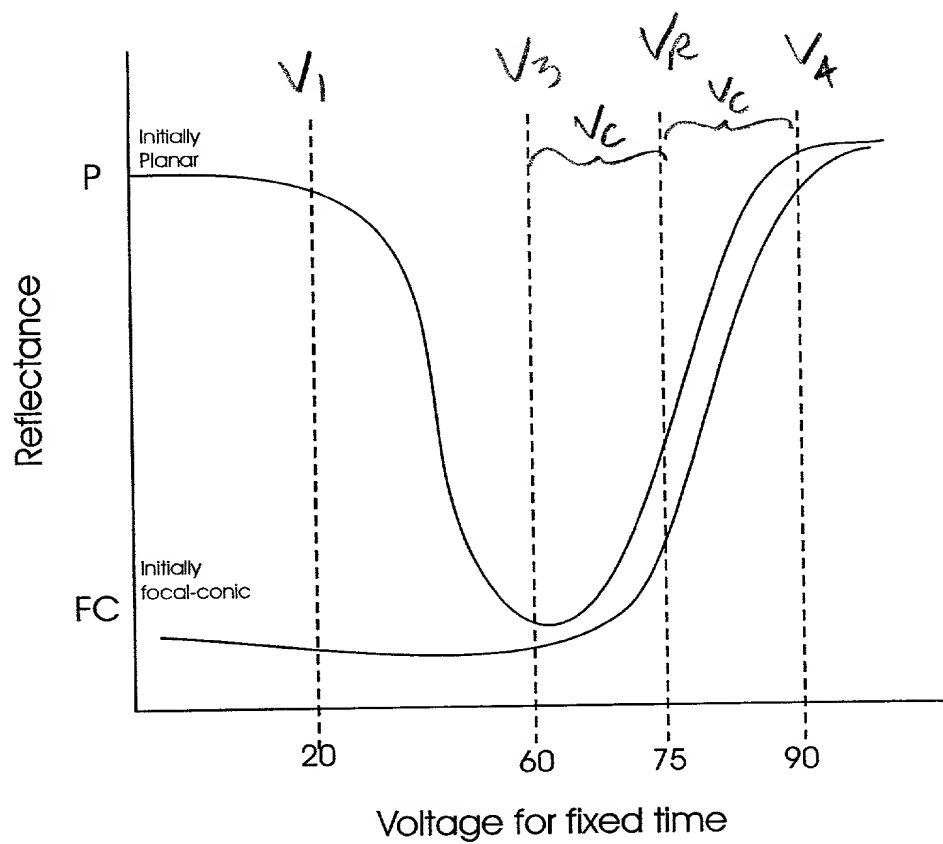


FIG. 4

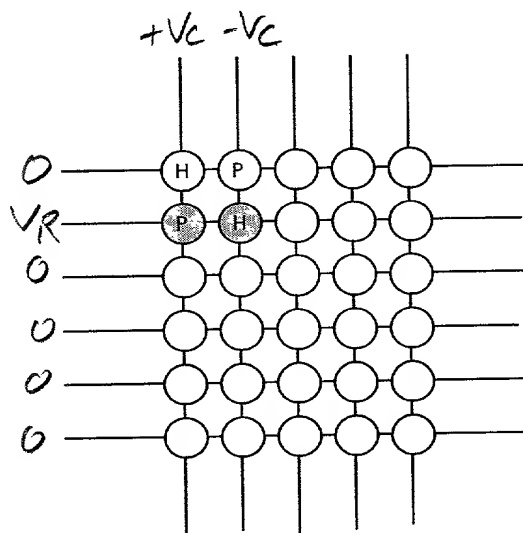


FIG. 5

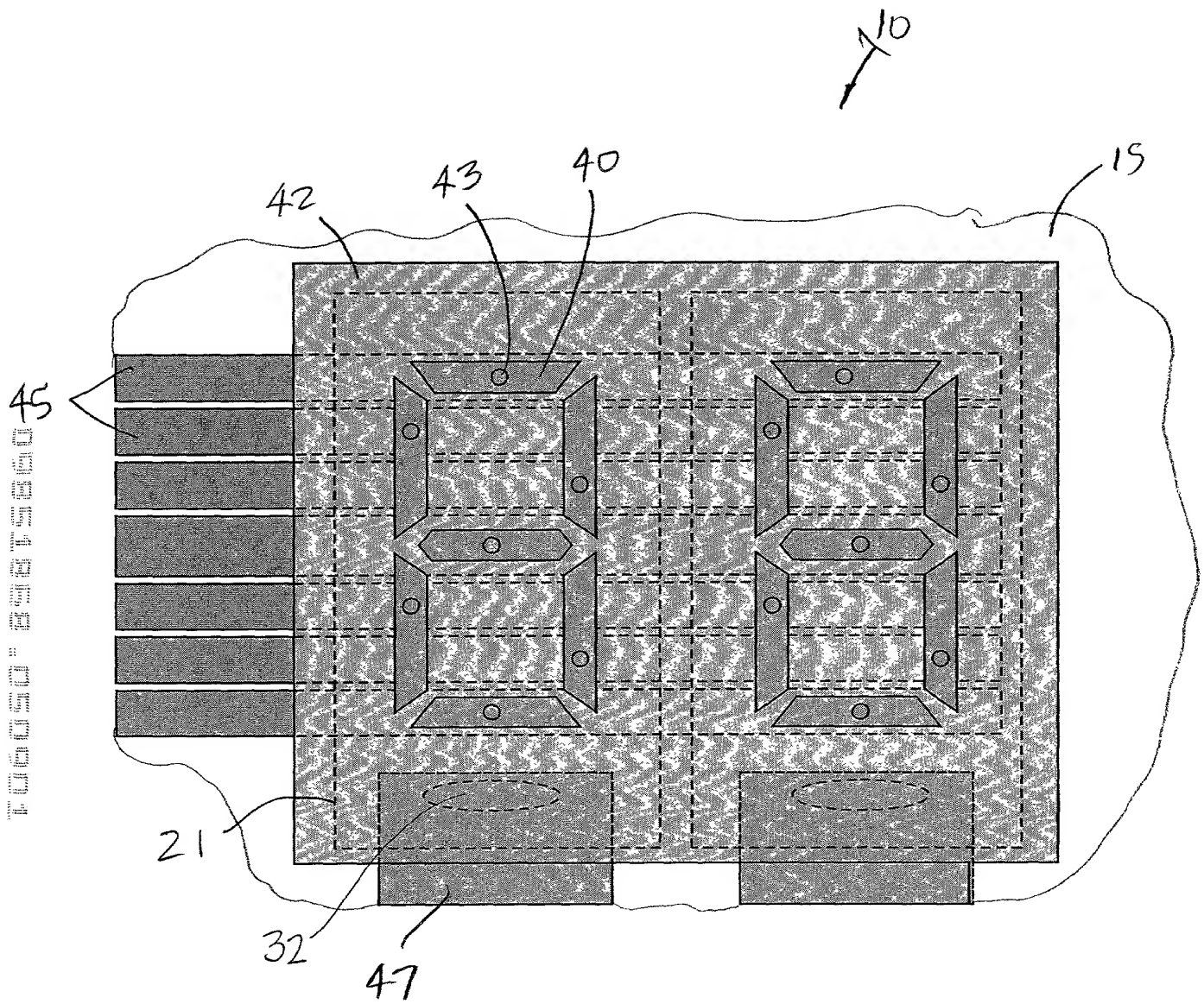


FIG. 6

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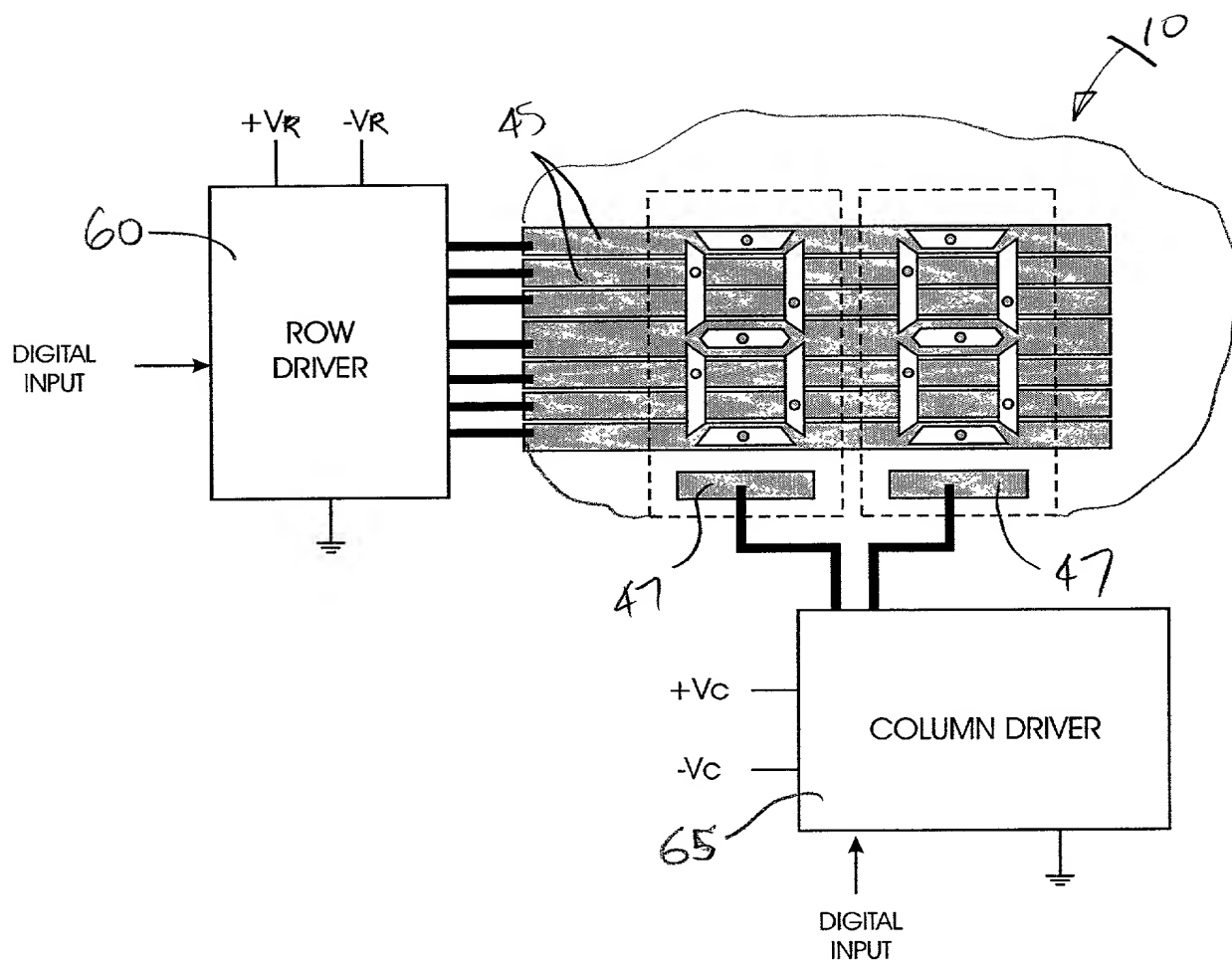


FIG. 7

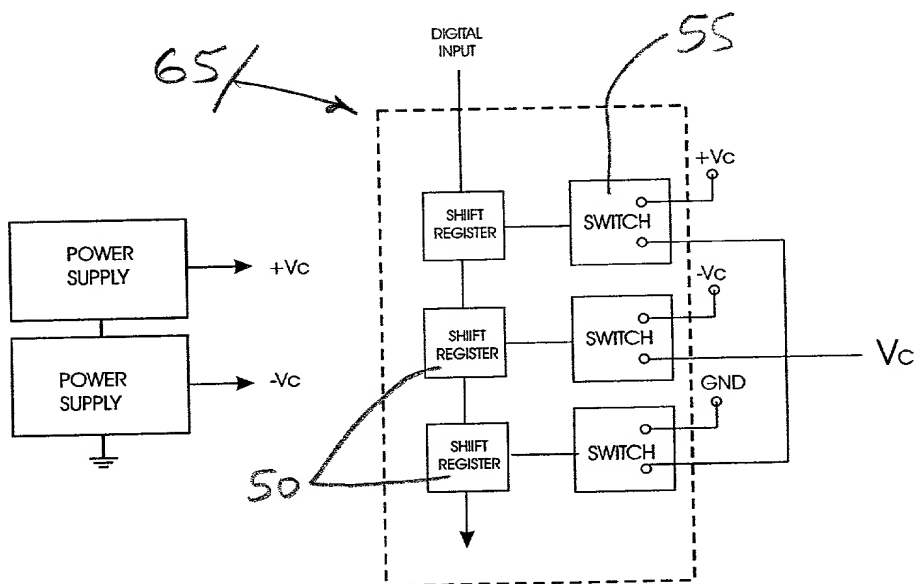
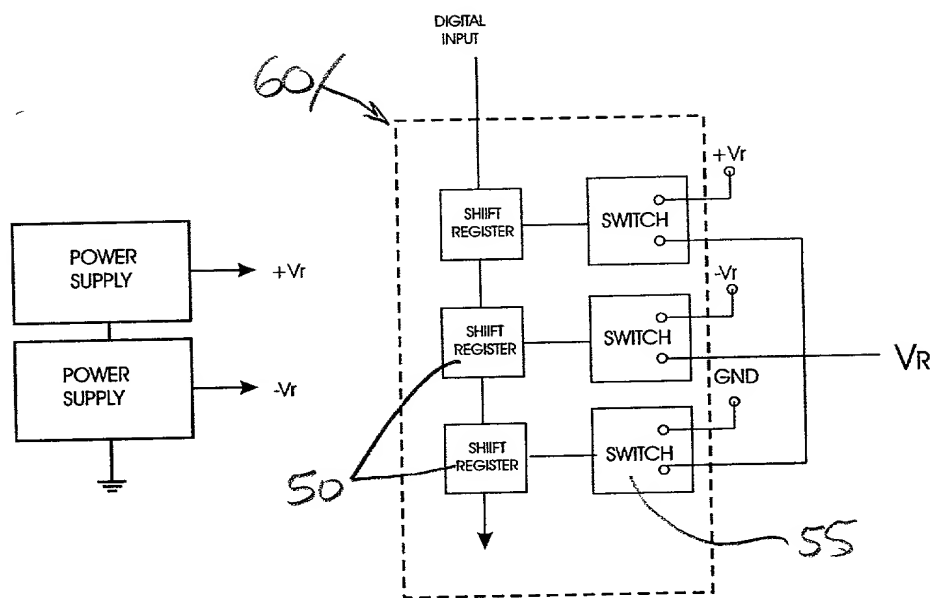


FIG. 8

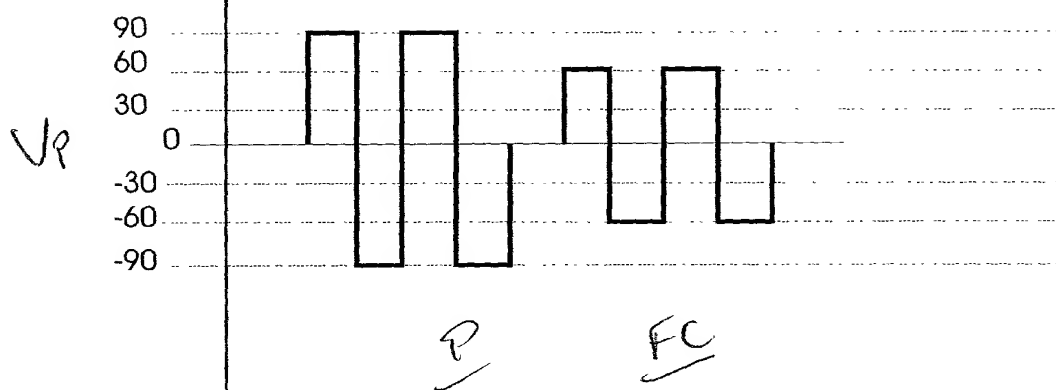
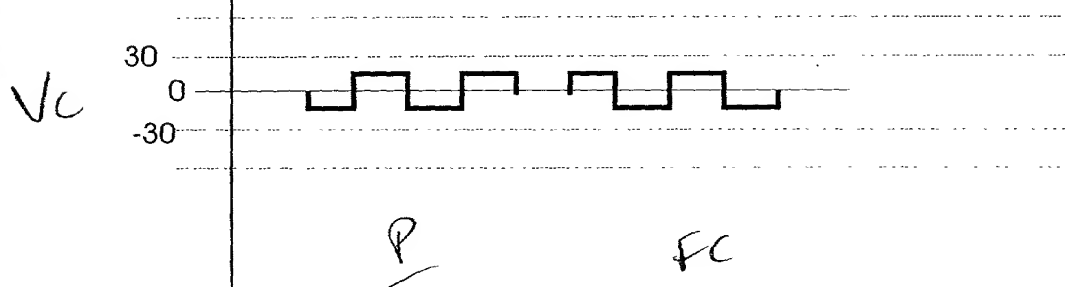
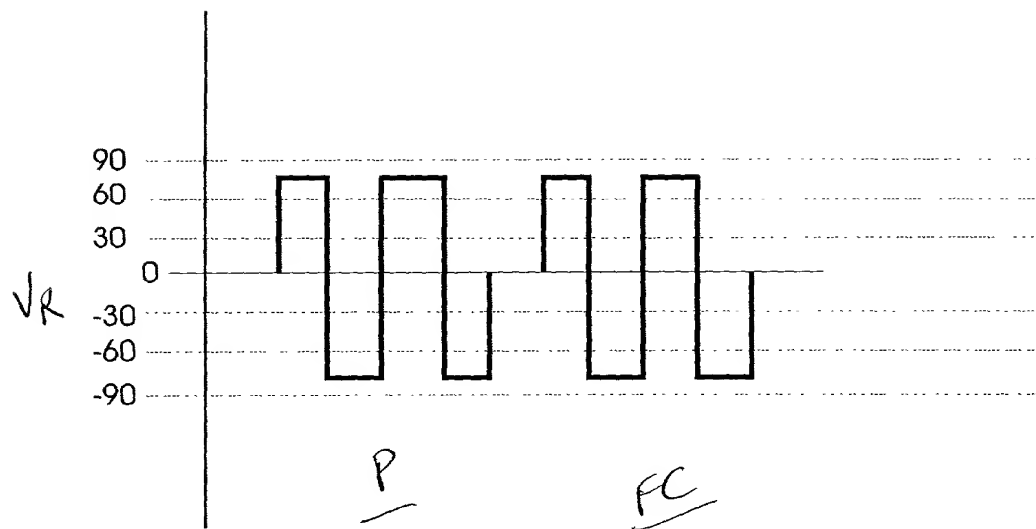


FIG. 9

The diagram shows a single driver chip 67 connected to a display panel 10. The chip 67 has a digital input and a Vsc supply input. It is connected to the panel 10 via a bus 45 and a signal line 47. The panel 10 shows a grid of pixels with horizontal and vertical electrodes.

FIG. 10





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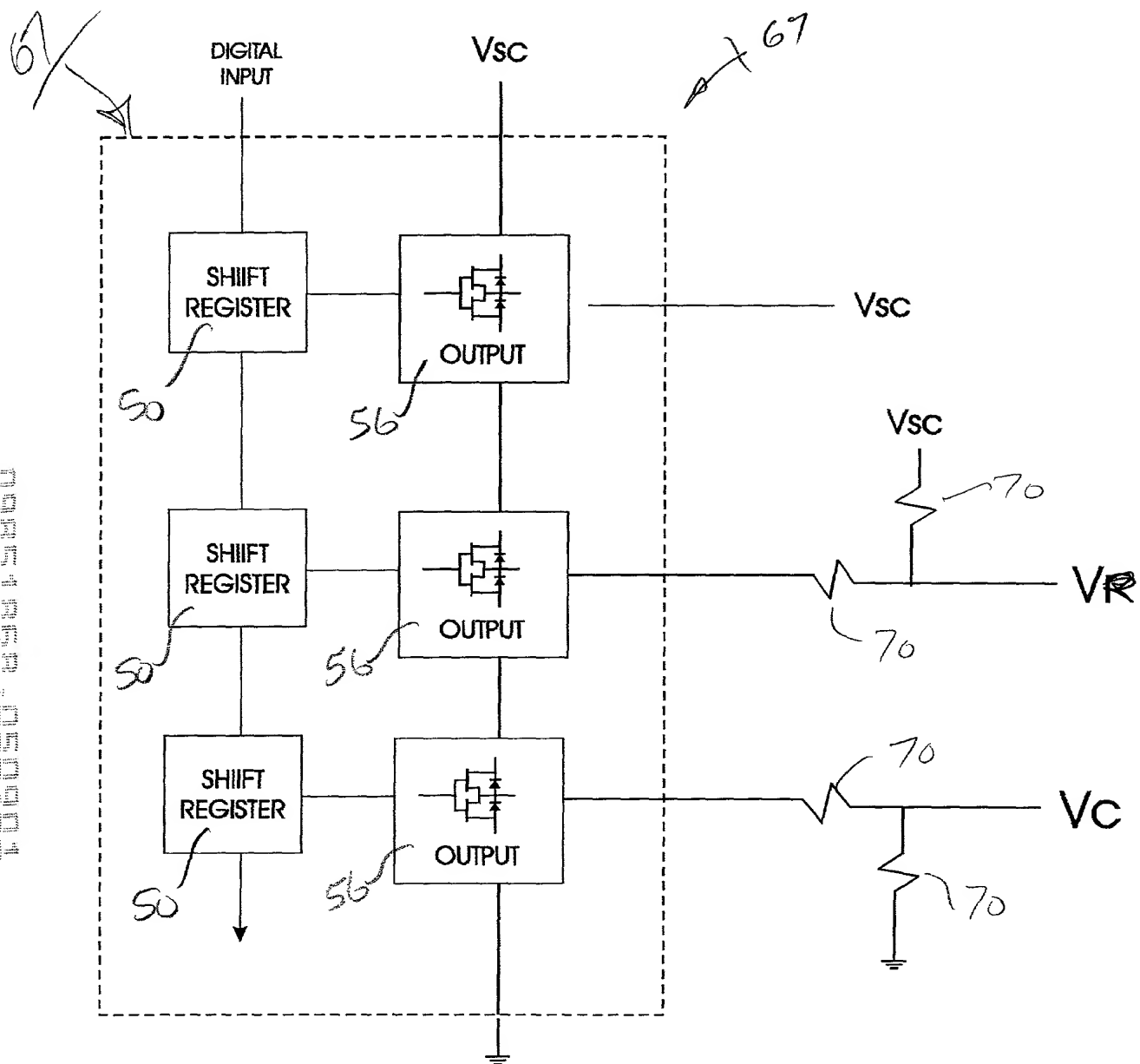


FIG. 12

0001850-000001

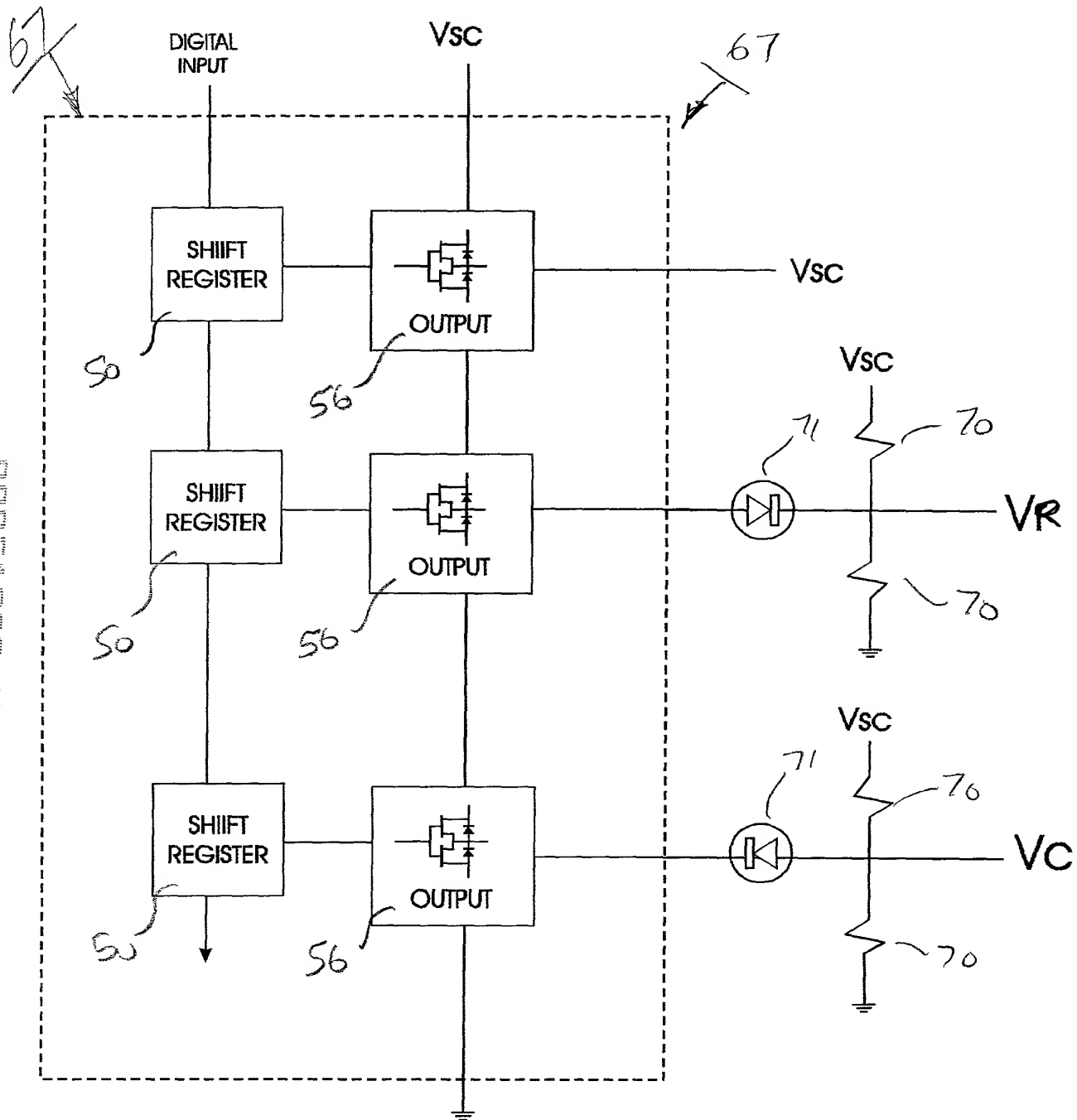


FIG. 3